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INVERSION AND ACCUMULATION LAYER FORMATION AT ELEVATED TEMPERATURES IN nGaAs-ANODIC OXIDE MIS DEVICES

FINAL TECHNICAL REPORT

LEVEL II

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ABSTRACT

At room temperature nGaAs-anodic oxide MIS devices typically exhibit some form of deep-depletion mode operation which is characteristic of a low thermal generation rate for minority carriers in the semiconductor. In addition, for accumulation mode bias voltages the small signal capacitance often does not approach the oxide capacitance, instead exhibiting a dispersion whereby this capacitance varies with the frequency of the a-c signal and the sweep-rate of the d-c bias voltage.

In this paper, capacitance-voltage measurements are reported for nGaAs-anodic oxide MIS devices taken at elevated temperatures with varying d-c bias voltage sweep rates. The formation of a stable inversion layer even at high sweep rates and the elimination of accumulation capacitance dispersion for a C-V measurement frequency of up to 1 MHz is observed at temperatures above room temperature. At high temperatures and slow sweep-rates, considerable mobile ion motion in the oxide is observed. A discussion of this observation based on recently developed theories for oxide growth is presented.

INTRODUCTION

There has been considerable recent interest in the growth and properties of oxide films on GaAs [1-11] because of the potential technological implications for GaAs MIS devices and integrated circuits. Of the homomorphic and heteromorphic layers which have been investigated, the homomorphic layers formed by anodic oxidation of GaAs have been of particular interest because this is one of the possible ways of achieving a "native" oxide analogous to that for the silicon-silicon dioxide system. While the study of the GaAs-anodic oxide interface and resulting device structures has lead to a better understanding of this materials system, the picture is still incomplete. Electrical measurements made at room temperature on GaAs-anodic oxide MIS devices show major deviations from the familiar behavior of the Si-SiO_2 system. Capacitance-voltage (C-V) measurements and photovoltage-derived measurements made on n-GaAs samples show considerable discrepancies in the zero-bias surface potential [7,12-14]. At room temperature the n-GaAs surface is very difficult to invert with an anodically grown oxide, and typically an nGaAs-anodic oxide MIS device exhibits some form of deep depletion mode characteristic [12-15], which is indicative of an inadequate minority carrier thermal generation rate in the semiconductor [16]. An anamolous dispersion of the accumulation mode capacitance is also observed in these devices [12], which is manifested by a frequency-dependent capacitance and a difficulty in achieving the oxide capacitance in accumulation, especially at high frequencies.

This paper describes results obtained on nGaAs-anodic oxide MIS structures at room temperature and elevated temperatures up to 200°C for varying sweep rates for the d-c bias voltage during C-V and conductance-voltage (G-V) measurements. Stable inversion layers are formed in these devices for temperatures above approximately 100°C. The disappearance of accumulation mode capacitance dispersion also occurs at these elevated temperatures. After the inversion layer is formed then as temperature is increased the inversion layer capacitance increases as expected [17]. It is also observed that the flat-band voltage shifts towards more negative values as the temperature is raised. Further, C-V measurements at high temperatures show clockwise hysteresis for fast sweep-rates, and counter-clockwise hysteresis for slow sweep-rates, indicative of ion motion in the oxide [18]. From the examination of this data at elevated temperatures it appears that the nGaAs-anodic oxide MIS system is not as dissimilar to the Si-SiO_2 system as an examination of the room temperature data alone would suggest.

EXPERIMENTAL PROCEDURES

The material used in this study was n-type GaAs of (100) orientation, having carrier concentrations of nominally $7 \times 10^{15} cm^{-3}$ (undoped), $3 \times 10^{16} cm^{-3}$ (undoped), and $1 \times 10^{17} cm^{-3}$ (Te-doped). Before anodization, the samples were chemically-mechanically polished, degreased, and etched by standard techniques [19]. The anodization solution was the same as that described by Hasegawa and Hartnagel [1] with the pH adjusted to 5.5.

Platinum was used as the cathode during anodization, and the electrolyte was continuously stirred during growth. All the oxides grown for this work were grown under illumination from a microscope lamp. Anodization current densities of 300, 400, and 500 $\mu amp/cm^2$ were used, with no significant changes in material or interface properties.

After oxide growth, an ohmic back contact of Indium was evaporated on the GaAs. The oxides were then annealed in ultra-high purity nitrogen at a temperature of 350°C for thirty minutes. This "drying" procedure has been used previously [7], and work is now in progress to study other annealing procedures, such as hydrogen annealing [20]. After annealing, top field plate contacts of Aluminum dots (~0.38 mm diameter) were evaporated. The anodization rate resulting from these experiments is approximately 18.2 $\mathring{A}$/volt, similar to results obtained by others [7,21]. The dielectric constant of the oxides were determined to be 8.2 and the breakdown strengths ranged from $(2.5\text{-}5)\times10^6$ volt/cm, for the various oxides grown in this study. The C-V measurements were taken using a PAR model 410 C-V plotter along with accompanying external circuitry to allow fast bias sweep rates. The C-V curves were displayed on an oscilloscope or an X-Y recorder, whichever was appropriate.

RESULTS

Since this paper attempts to establish the existence of an inversion layer and the elimination of capacitance dispersion at elevated temperatures, some preliminary remarks are in order. First of all, the substrate carrier

concentrations were established by Hall effect measurements but they were not measured on each sample. Thus the carrier concentrations quoted are nominal values and small variations in these values are possible from sample to sample. Secondly, an anodization constant of 18.2 Å/V was established by ellipsometry measurements and confirms many previous results [7,21]. This number was used throughout the remainder of the experiments to determine film thickness, since the thickness was not measured on each sample. Also, a color chart was obtained [22], which agreed with our measurement of the film thickness, and which gave a reasonable check of the thickness from run to run.

Initially, it was found that for an accumulation mode voltage of +10V, the MIS capacitance approached a constant value as the sample temperature was raised above 100-150°C for all substrate resistivities and for a measurement frequency of 1 MHz. Assuming this capacitance to be the oxide capacitance and that there was no dispersion under these conditions resulted in a low frequency dielectric constant of 8.2 at 1 MHz to within 2-3% for the many samples examined. Furthermore, C-V measurements taken at 1 kHz at room temperature yielded the same dielectric constant for each substrate resistivity and for a wide range of oxide film thicknesses (750Å - 1500Å) grown and studied on substrates with these resistivities. It is generally considered that a C-V measurement frequency of 1 kHz is low enough to eliminate dispersion for strong accumulation mode voltages [15,23]. The agreement between the 1 MHz MIS capacitance at elevated temperatures (greater than about 100°C) and the 1 kHz room temperature capacitance, both measured at an accumulation mode voltage

of +10 volts, and the agreement between the dielectric constants obtained from these capacitances for a wide range of substrate resistivities and oxide film thicknesses is taken as partial justification for assuming the elimination of capacitance dispersion at elevated temperatures. The remainder of the justification will be illustrated from the nature of the high temperature 1 MHz C-V curves. If this constant, frequency independent capacitance at high temperatures is the true oxide capacitance, as it seems to be, then one can calculate the minimum capacitance at a given doping level which would result from a completely formed inversion layer. The value of the calculated minimum capacitance will be shown on subsequent C-V curves, and this calculation will be subject to the small experimental errors in the substrate doping level and oxide film thickness noted above.

Figure 1 shows C-V characteristics taken at 1 MHz for an anodic oxide grown on a GaAs substrate having an electron concentration of $1x10^{17}cm^{-3}$, for temperatures of 50°C, 100°C, 150°C, and 200°C. The bias sweep rate was 400 V/sec (±10 volts in 100 msec). Here it can be remarked that, as far as can be ascertained, the room temperature C-V characteristics observed in this study are very similar to those reported by other authors [7,12-15,23]. The oxide capacitance and resulting calculated inversion layer capacitance are indicated on each figure. At 50°C, the depletion mode behavior for negative bias voltages and the capacitance dispersion is still very much prevalent. At 100°C, the oxide capacitance is obtained in accumulation and there is a tendency for the C-V curves to indicate an inverted surface on the bias voltage

after the deep depletion mode has been formed at large negative bias voltages. At 150°C the capacitance is constant for voltages less than -4 volts at the value required [17] for inversion layer formation, and is maintained constant at voltages of -20 volts. If the bias voltage sweep-rate was lowered, then the formation of the inversion layer was seen to occur at even lower temperatures. This is to be expected [24]. As the temperature is further raised, the accumulation and inversion conditions are maintained, and the flatband voltage shifts toward negative values with increasing temperature, as shown in Figure 1(d). This phenomena is observed in the $Si-SiO_2$ system dominated by fast surface states [25]. After the inversion layer was formed, the temperature dependence of the MIS capacitance for strong inversion mode bias voltages (-10 volts) was studied. This temperature dependence obeyed the theoretical equation for the minimum capacitance given by Sze [17,p.437] to within the experimental measurement accuracy discussed at the beginning of this section.

The fact that a flat-band condition was achieved in these devices was further verified from conductance-voltage (G-V) measurements. At temperatures below 100°C, the small-signal conductance does not exhibit a maximum as expected [17]. However, above 100°C, the G-V measurements do exhibit a maximum conductance, and this maximum shifts toward more negative voltages as the temperature increases in the same manner as the C-V curves. Thus, from the data presented here it appears that at high temperatures the formation of an inversion layer does occur, that the capacitance dispersion at frequencies up to 1 MHz is eliminated, and that the Fermi-level pinning which may occur in nGaAs-anodic oxide MIS structures at room temperature [13] does not occur above about 100°C.

For completeness, Figures 2 and 3 show additional data supporting the above conclusions taken on devices with substrate carrier concentrations of $3x10^{16}cm^{-3}$ and $7x10^{15}cm^{-3}$. Some additional general conclusions which can be drawn from this data are that the lower the substrate carrier concentration the higher the temperature required to substantially reduce high frequency capacitance dispersion. Also, at a given temperature, say 150°C, the transition from accumulation to depletion seems to be more abrupt the lower the substrate carrier concentration for a given set of experimental conditions. There does not seem to be any correlation between the temperature required to achieve inversion and the substrate carrier concentration. While these observations are possible from the data, it is premature to draw conclusions from them at this time. Further work is in progress to carefully examine several aspects of the high temperature C-V and G-V data.

Figure 4 shows the effect of bias voltage sweep rate on the C-V curves at a substrate temperature of 200°C. At near room temperature the hysterisis of the C-V curves is always clockwise, usually indicative of charge injection into the oxide [18]. In a future paper we will present additional data in support of this conclusion. However, at temperatures above 150°C, the C-V curve hysterisis is clockwise for high sweep rates (greater than about 2-3 Hz for the ±10 volt bias sweep) and counter-clockwise for slower sweep rates (less than 1 Hz for the ±10 volt bias sweep) indicative of ion motion in the oxide [18]. We feel that it is quite possible that the counter-clockwise hysterisis can be attributed to the presence of excess As ions at the oxide-semiconductor interface.

Coleman et al. [10] have concluded that Ga and As are mobile ions in the anodic oxide and Chang et al. [26] have used Auger analysis to conclude that there is an excess As concentration at the interface. In our experiments at elevated temperatures, when the voltage sweep was restricted to positive values, the clockwise hysterisis remained for all sweep rates. For negative voltage sweeps the hysterisis was counter-clockwise for slow sweep rates and clockwise for high sweep rates. This is taken as evidence that the species responsible for the counter-clockwise hysterisis shown in Figure 4 are positive ions present at the oxide-semiconductor interface and not uniformly distributed throughout the oxide. This also is a topic under further investigation.

CONCLUSIONS

Capacitance-voltage measurements have been presented for nGaAs-anodic oxide MIS devices. The data shows that a stable inversion layer can be formed on the GaAs surface for temperatures above approximately 100°C for a wide range of substrate doping levels. At these elevated temperatures, the capacitance dispersion in the accumulation mode is also eliminated, and at temperatures near 150°C and above the nGaAs-anodic oxide interface behaves in a manner which is related in its general features to the $Si-SiO_2$ system. A more detailed study of the high temperature electrical properties of anodic oxides on GaAs can lead to a better understanding and elimination of some of the problems which are prevalent at room temperature.

ACKNOWLEDGMENTS

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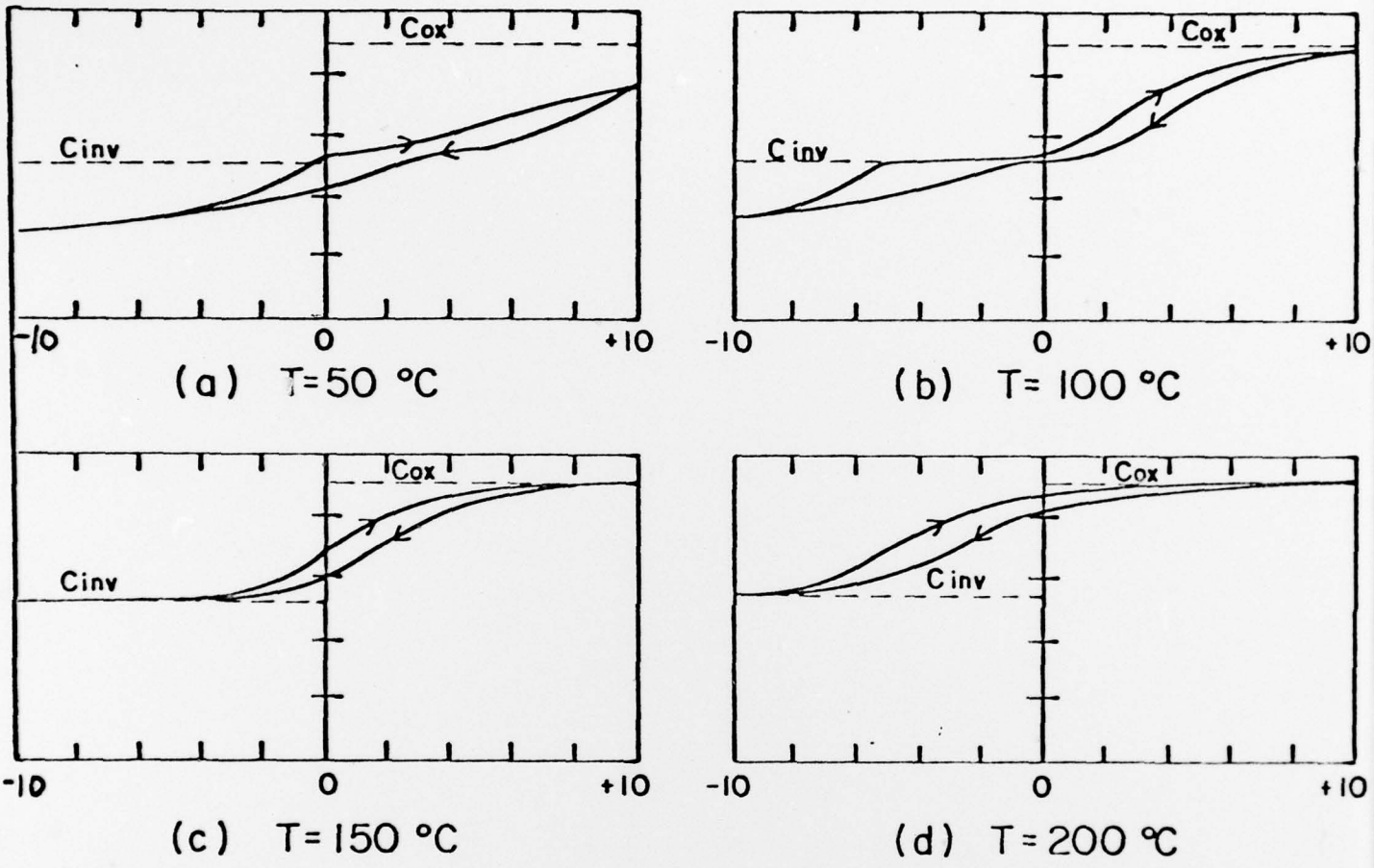
LIST OF FIGURES



HORIZONTAL SCALE : 2 volts / division
VERTICAL SCALE: 20 pf / division

Fig. 1

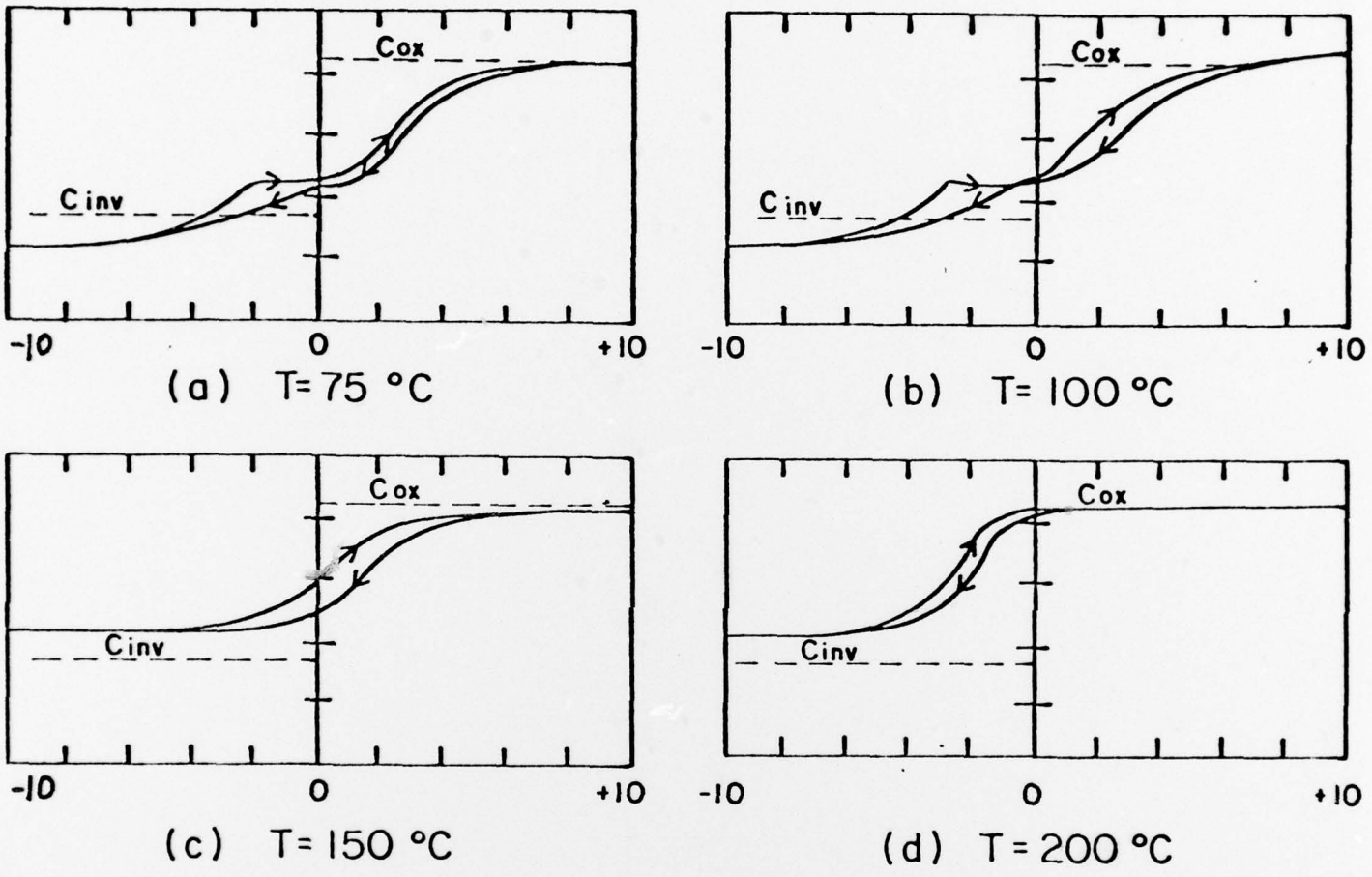


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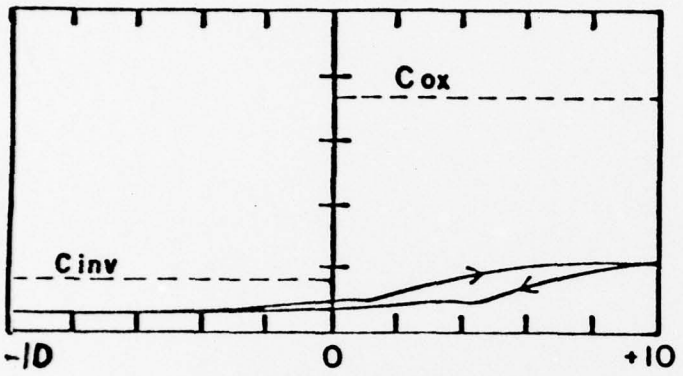
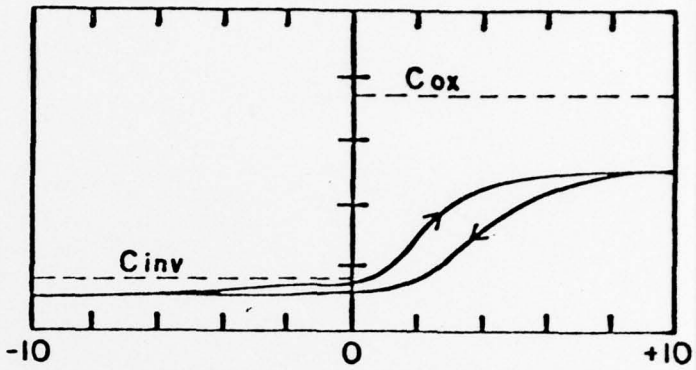
Fig. 2



(a) T=50 °C



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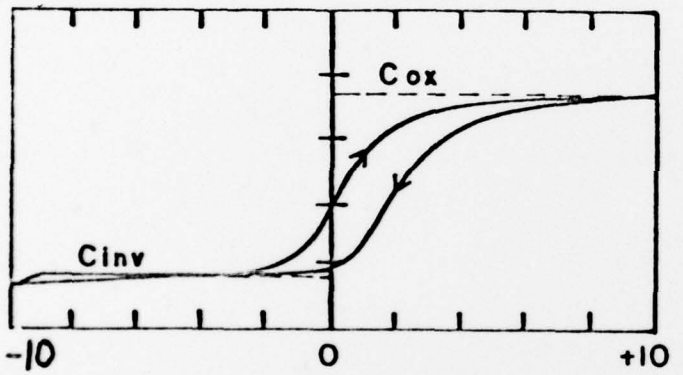

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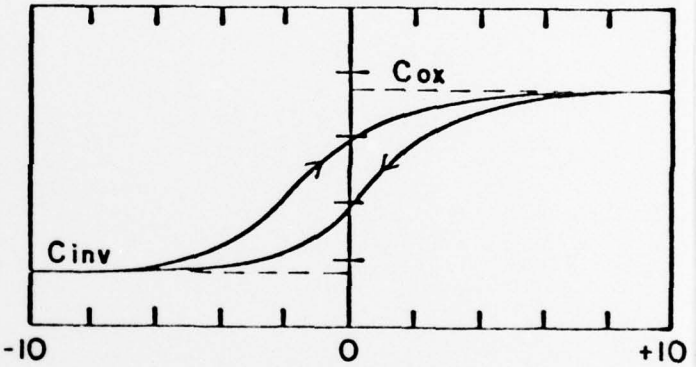
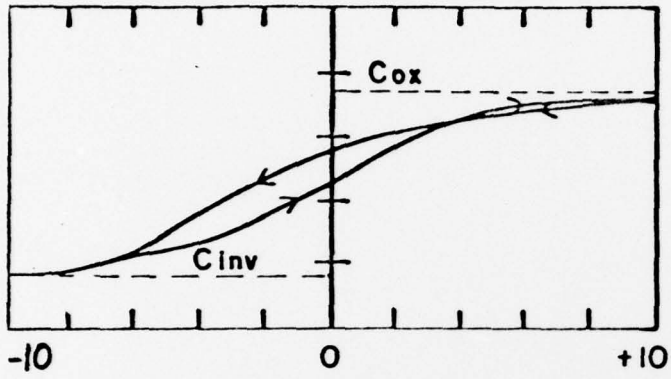
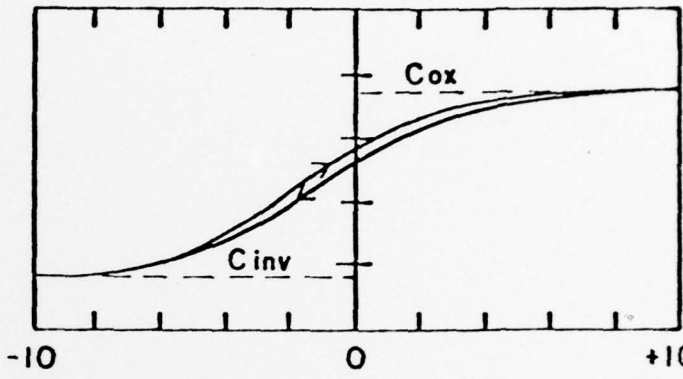


(d) T=200 °C

HORIZONTAL SCALE : 2 volts / division
VERTICAL SCALE : 20 pf / division



(a) T=200 °C



(b) T=200 °C

HORIZONTAL SCALE : 2 volts / division
VERTICAL SCALE : 20 pf / division

Fig. 4

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

At room temperature nGaAs-anodic oxide MIS devices typically exhibit some form of deep-depletion mode operation which is characteristic of a low thermal generation rate for minority carriers in the semiconductor. In addition, for accumulation mode bias voltages the small signal capacitance often does not approach the oxide capacitance, instead exhibiting a dispersion whereby this capacitance varies with the frequency of the a-c signal and the sweep-rate of the d-c bias voltage.

In this paper, capacitance-voltage measurements are reported for nGaAs-anodic

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oxide MIS devices taken at elevated temperatures with varying d-c bias voltage sweep rates. The formation of a stable inversion layer even at high sweep rates and the elimination of accumulation capacitance dispersion for a C-V measurement frequency of up to 1 MHz is observed at temperatures above room temperature. At high temperatures and slow sweep-rates, considerable mobile ion motion in the oxide is observed. A discussion of this observation based on recently developed theories for oxide growth is presented.